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EXAMINER	
MEONSKE, TONIA L	
ART UNIT	**PAPER NUMBER**
2183	

DATE MAILED: 09/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/054,577	MOYER, WILLIAM C.	
	Examiner	Art Unit	
	Tonia L Meonske	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 March 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 November 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/13/01, 3/17/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. It is the same figure as Fig. 1 in US Pat. 5,923,893. (Moyer et al.) See MPEP § 608.02(g).

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the following limitations must be shown or the features canceled from the claims. No new matter should be entered.

a. Claim 6: "A method for a first processor, coupled to a second processor via a coprocessor communication bus, to selectively alter an execution mode of said first processor, comprising: ... selectively altering the execution mode of said first processor in response to the region indicator."

b. Claim 7: "The method of claim 6, wherein altering the execution mode of said first processor comprises altering a functionality of said first processor."

c. Claim 8: "A method for a first processor, coupled to a second processor via a coprocessor communication, to selectively alter an execution mode of said first processor, comprising:...selectively altering the execution mode of said first processor in response to the region specifier."

d. Claim 17: "The processor of claim 15, wherein each region storage device comprises a base location storage device and a mask storage device to define each broadcast region."

e. Claim 19: "...selectively providing said operand to be written to said one of the plurality of registers during said write operation based on the current execution region."

f. Claim 20: "...wherein each execution region within the set of execution regions has a corresponding region storage device for defining the execution region."

3. Corrected drawing sheets are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

4. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

5. The applicant is requested to submit a "Brief Summary of Invention". See MPEP 608.01(d).

6. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Objections

7. Claim 18 recites the limitation "the compare circuitry" in line 12 of the claim. There is insufficient antecedent basis for this limitation in the claim. See MPEP 2173.05(e). The examiner notes, that upon further examination, the compare circuitry will be interpreted to be the execution region control unit.

8. Claims 19 and 20 are objected based on their dependency to Claim 18.

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

10. Claims 1 – 5 and 9 are rejected under 35 U.S.C. 102(b) as being anticipated by Borkar et al., Supporting Systolic and Memory Communication in iWarp,1990, ACM Sigarch Computer Architecture News, Proceedings of the 17th Annual International Symposium on Computer Architecture (herein after "Borker et al.").

11. Referring to claim 1, Borkar et al. have taught a method for a processor (Page 1, 1. Introduction, second paragraph, "The iWarp processor..."/ The iWarp processor is a processor.) having a register file comprising a plurality of registers(Page 1, 1. Introduction, Figure 2, Multi-ported Register File) and a broadcast specifier corresponding to the register file, (Page 7, 5.3

Dynamic assignment of queue destinations, second column, "A cell that wants to send locally generated data to another cell deposits the data into one of the queues allocated for internal use and then assigns an output logical channel to this queue, as shown in Cell 0 of Figure 7." Page 10, 7.1 Data interface to the computation agent, first paragraph/ A set of message queues (Page 7, Table 1) is the broadcast specifier. An output systolic gate is a register that has the ability to transmit data to another cell. (See Page 1, 1. Introduction, Figure 1 for definition of cell). The output systolic gate is found in the register address space, and thus the register file. The output systolic gate uses a message queue with an internal source to transmit data to a different cell. This message queue is found in the set of message queues, the broadcast specifier. Therefore, the broadcast specifier, the set of message queues, corresponds to the register file because the output systolic gate, a register, uses a message queue.) to selectively broadcast via a coprocessor communication bus, (Page 4, 3.2 Logical channels, Page 4, 3.2.1. Increasing connectivity, first paragraph, Page 6, 5.1 Queues and logic channels, second paragraph, Page 6, 5.2 Static allocation of queue sources, third paragraph, Page 6 , 5.3 Dynamic assignment of queue destinations, first paragraph, second paragraph, Page 6, Figure 7/ A message queue with an external source is a logical channel. The coprocessor communication bus is the set of logical channels, implemented by the physical channels. To selectively broadcast via a coprocessor communication bus is to select an output logical channel to transmit data to a different cell.) write transactions to said register file (Page 3, 3.1.1. Program access to data in communication, first paragraph/ A write to a gate, a register in the register space, or register file, is a write transaction to said register file. The gate is also known as an output systolic gate.), the method comprising:

a. receiving an operand to be written to said register file(Page 10, 7.1 Data interface to computation agent, second paragraph/ Receiving an operand to be written to said register file is receiving the result of the arithmetic operation from the instruction execution that will be written to an output systolic gate.)

b. selecting one of said plurality of registers in said register file; (Page 10, 7.1 Data interface to computation agent, first paragraph, second paragraph/ There are two output systolic gates in the register address space, or register file, which can serve as result registers of an instruction. The instruction specifies, or selects, the output systolic gate that will be the result register. Each output systolic gate is one of a plurality of registers in said register file.)

c. selectively providing via said coprocessor communication bus said operand to be written in said register file based on the broadcast specifier. (Page 10, 7.1 Data interface to computation agent/ The said operand written in said register file is the operand written into the result register, which is an output systolic gate. After writing the operand to the result register, the result is queued in a message queue for transmission to another cell. Selectively providing via said coprocessor communication bus said operand is the transmission of the operand from one source cell to the destination cell. The result enters and is eventually transmitted from one message queue selected from the broadcast specifier, the set of message queue. The destination of the transmission is based on the message queue selected.)

12. Although Borkar et al. teach instructions using output systolic gates as result registers (Page 10, 7.1 Data interface to computation agent), Borkar et al. is silent about providing to said

register file said operand to be written to said register file. However, this feature is deemed to be inherent to the Borkar et al. system because operands are written to the output systolic gate, a register. The data must be provided to the register file in order for it to be written to the output systolic gate. The Borkar et al. system would be inoperative if the operand is not provided to the register file because it would not be able to write the operand to the output systolic gate.

13. Referring to claim 2, Borkar et al. have taught the method of claim 1, as described above, and wherein the broadcast specifier comprises a set of broadcast indicators, each broadcast indicator within the set of broadcast indicators corresponding to one of the plurality of registers. (Page 6 - 7, 5.3 Dynamic assignment of queue destinations, Page 10, 7.1 Data interface to computation agent, first paragraph, Page 7, Table 1/ The broadcast specifier is the set of message queues. The individual message queues with an internal source are broadcast indicators and comprise the broadcast specifier. The queues that have an internal source that correspond to the output systolic gates, which are registers, are the set of broadcast indicators corresponding to one of the plurality of registers.)

14. Referring to claim 3, Borkar et al. have taught the method of claim 2, as described above, and wherein selectively providing via said coprocessor communication bus said operand to be written in said register file is based on the broadcast indicator corresponding to the selected one of said plurality of registers in said register file. (Page 10, 7.1 Data interface to computation agent, Page 7, 5.3 Dynamic assignment of queue destinations, "A cell that wants to send locally generated data to another cell deposits the data into one of the queues allocated for internal use and then assigns an output logical channel to this queue, as shown in Cell 0 of Figure 7." / Said operand to be written in said register file is the operand written to the result register, which is an

output systolic gate, after an arithmetic operation. Selectively providing via said coprocessor communication bus said operand to be written in said register file is the transmission of the operand from one source cell to the destination cell. The operand is placed in a message queue with an internal source corresponding to an output systolic gate. This message queue is a broadcast indicator. Therefore, the transmission of the operand (selectively providing via said coprocessor communication bus said operand to be written in said register file) is based upon a message queue with an internal source that corresponds to an output systolic gate (the broadcast indicator corresponding to the selected one of said plurality of registers in said register file).)

15. Referring to claim 4, Borkar et al. have taught the method of claim 1, as described above, and wherein the broadcast specifier is one of a plurality of broadcast specifiers within the processor, each of the plurality of broadcast specifiers corresponding to at least one broadcast region of the processor. (Page 5, Figure 4, Page 6 – 7, 5.3 Dynamic assignment of queue destinations, Page 7, Table 1/ A broadcast specifier is a set of message queues. There are five possible destinations (XLeft (XL), XRight (XR), YUp (YU), YDown (YD), Internal (I)). The destinations are the broadcast regions of the processor. Thus there are five sets of message queues (plurality of broadcast specifiers), each set with its own destination (corresponding with at least one broadcast region of the processor))

16. Referring to claim 5, Borkar et al. have taught the method of claim 4, as described above, and further comprising:

a. selectively providing, via said coprocessor communication bus, a region indicator corresponding to a current broadcast region of a current write transaction. (Page 10, 7.1 Data interface to computation agent, Page 8, 6.1 The reservation pool/ After writing the

operand of an arithmetic operation to the result register (current write transaction), which is an output systolic gate, the result is queued in a message queue for transmission to another cell. Intercell communication connects pathway segments to route data between cells. Pathway begin markers (a region indicator) specify the route of the pathway (current broadcast region) and destination of the data. The pathway segments are logic channels, which are implemented on a physical bus. (Page 4, 3.2.1. Increasing connectivity) The transmission of the operand and pathway begin marker from one cell to another cell is selectively providing, via a coprocessor communication bus, a region indicator corresponding to a current broadcast region of a current write transaction.)

17. Referring to claim 9, Borkar et al. have taught a method for a processor, (Page 1, 1. Introduction, second paragraph, "The iWarp processor..."/ The iWarp processor is a processor.), having a register file comprising a plurality of registers, (Page 1, 1. Introduction, Figure 2, Multi-ported Register File) to selectively broadcast via a coprocessor communication bus, (Page 4, 3.2 Logical channels, Page 4, 3.2.1. Increasing connectivity, first paragraph, Page 6, 5.1 Queues and logic channels, second paragraph, Page 6, 5.2 Static allocation of queue sources, third paragraph, Page 6, 5.3 Dynamic assignment of queue destinations, first paragraph, second paragraph, Page 6, Figure 7/ A message queue with an external source is a logical channel. The coprocessor communication bus is the set of logical channels, implemented by the physical channels. To selectively broadcast via a coprocessor communication bus is to select an output logical channel to transmit data.) write transactions to said register file (Page 3, 3.1.1. Program access to data in communication, first paragraph/ A write to a gate, or register in the register space, or register file,

is a write transaction to said register file. The gate is also known as an output systolic gate.), the method comprising:

a. receiving an operand to be written to said register file; (Page 10, 7.1 Data interface to computation agent, second paragraph/ Receiving an operand to be written to said register file is receiving the result of the arithmetic operation from the instruction execution that will be written to an output systolic gate.)

b. selecting one of said plurality of registers in said register file; (Page 10, 7.1 Data interface to computation agent, first paragraph, second paragraph/ There are two output systolic gates in the register address space, or register file, which can serve as result registers of an instruction. The instruction specifies, or selects, the output systolic gate which will be the result register. The output systolic gates is one of a plurality of registers in said register file.)

c. selectively providing via said coprocessor communication bus said operand to be written in said register file. (Page 10, 7.1 Data interface to computation agent/ The said operand written in said register file is the operand written into the result register, which is an output systolic gate. After writing the operand to the result register, the result is queued in a message queue for transmission to another cell. Selectively providing via said coprocessor communication bus said operand is the transmission of the operand from one source cell to the destination cell.)

18. Although Borkar et al. teach instructions using output systolic gates as result registers (Page 10, 7.1 Data interface to computation agent), Borkar et al. is silent about providing to said register file said operand to be written to said register file. However, this feature is deemed to be

inherent to the Borkar et al. system because operands are written to the output systolic gate, a register. The data must be provided to the register file in order for it to be written to the output systolic gate. The Borkar et al. system would be inoperative if the operand is not provided to the register file because it would not be able to write the operand to the output systolic gate.

19. Although Borkar et al. teaches selectively providing via said coprocessor communication bus said operand to be written in said register file, Borkar et al. is silent about [selectively providing via said coprocessor communication bus said operand to be written in said register file] based on a current execution region of said processor. However, this feature is deemed to be inherent because the cells in iWarp are programmed individually with explicit communication directives, and thus each cell has its own program code to run. (Page 1 1.Introduction, second column, second paragraph, Page 2, 1.Introduction, first paragraph). Because there are explicit communication directives in the code, the transmission (selectively providing via said coprocessor communication bus said operand to be written in said register file) is based on the individual cell's program code (the current execution region of said processor). The Borkar et al. system would be inoperative if there was no code, and thus instructions, for the cells.

20. Claims 6 and 7 are rejected under 35 U.S.C. 102(b) as being anticipated by Borkar et al., iWarp: An Integrated Solution to High-Speed Parallel Computing, 1988, Proceedings of the 1988 ACM/IEEE conference on Supercomputing (herein after "iWarp").

21. Referring to claim 6, iWarp have taught a method for a first processor, coupled to a second processor via a coprocessor communication bus, (Page 332, 2.2 Forming iWarp systems, Figure 3(b)), to selectively alter an execution mode of said first processor, comprising:

a. receiving, via said coprocessor communication bus, a region indicator from said second processor, wherein the region indicator indicates a current execution region of the second processor; (Page 335, 4.2 Messages and Pathways, Page 336 – 337, 5.3 The pathway unit/ Pathway segments comprise the coprocessor communication bus. An open pathway marker sets up a pathway segment. The open pathway marker, the region indicator, contains the route to the destination cell, including the destination address. The destination address, found in the open pathway marker, indicates the current execution region of the second processor.)

b. selectively altering the execution mode of said first processor in response to the region indicator. (Page 337, 5.3 The pathway unit, "Upon the arrival of an open pathway marker, the pathway unit interprets the address to see if it is addressed to this cell, and, if so, posts an event to the computation agent to invoke the appropriate routine."/ The intermediate cell (first processor) invokes a routine, thus altering the execution mode, in response to the routing information in the open pathway marker.)

22. Referring to claim 7, iWarp have taught the method of claim 6, as described above, and wherein altering the execution mode of said first processor comprises altering a functionality of said first processor. (Page 337, 5.3 The pathway unit, "Upon the arrival of an open pathway marker, the pathway unit interprets the address to see if it is addressed to this cell, and, if so, posts an event to the computation agent to invoke the appropriate routine."/ The intermediate cell (first processor) invokes a routine, thus altering a functionality, in response to the routing information in the open pathway marker.)

23. Claim 8 is rejected under 35 U.S.C. 102(b) as being anticipated by Moyer et al. (US Pat. 5,923,893).

24. Referring to claim 8, Borkar et al. have taught a method for a first processor (Fig. 1, Coprocessor 14), coupled to a second processor (Fig. 1, Processor 12) via a coprocessor communication bus (Fig. 1, Coprocessor Interface 30), to selectively alter an execution mode of said first processor (Col. 5, lines 58 – 63, Col. 6, lines 30 – 32/ The coprocessor (first processor) selectively alters an execution mode of said first processor in response to the processor (second processor's) GPR when it has functions that overlay the processor's GPR.), comprising:

a. receiving, via said coprocessor communication bus, a register specifier from said second processor, (Fig. 3, Regwr* 67, Reg[4:0] 68, Col. 6, lines 14 – 22)/ Regwr* and Reg[4:0] are the register specifier. The signals are a part of Coprocessor Communication Bus 30 (coprocessor communication bus). They are sent by Processor 12 (the second processor), and received by Coprocessor 14.)

b. wherein the register specifier indicates a selected register within a register file of said second processor in which an operand is being written; and (Col. 6, lines 14 – 22/ Regwr* is asserted when the register is updated, or written. Reg[4:0] indicates the register number of the register, found in the register file, being updated. Reg[4:0] indicates a selected register within a register file of said second processor in which an operand is being written.)

c. selectively altering the execution mode of said first processor in response to the register specifier. (Col. 5, lines 58 – 63, Col. 6, lines 30 – 32/ The coprocessor (first processor) selectively alters an execution mode of said first processor in response to the

processor (second processor's) GPR when it has functions that overlay the processor's GPR.)

25. Claims 10-12 are rejected under 35 U.S.C. 102(b) as being anticipated by Parrish et al. (US Pat. 5,117,350).

26. Referring to claim 10, Parrish et al. have taught a processor, comprising:

a. a plurality of registers; (Col. 12, lines 36 – 43/ Fig. 6A, Memory 314/ The memory is divided into memory blocks, a plurality of registers.)

b. circuitry for performing a write operation to one of the plurality of registers (Col. 7, lines 51 – 60, Col. 11, lines 65 – 68, Col. 12, lines 1 – 5, 16 – 35, Fig. 6A, Memory 314, Address Translation Hardware 319, Addr, Din, Interconnect Bus 360, Bus Interface 317,Address 302, Data 304/ The write operation to one of the plurality of registers is the write transfer of data to distributed common memory, which is located in memory. A write transfer is issued to all copies of the shared memory. There is a write transfer to the local memory of the node that generated the initial write, and the local memory of the other participating nodes with a copy of the shared information. The circuitry for performing the write operation is the Interconnect Bus 360, Bus Interface 317, Address Translation Hardware 319, Address 302, Data 304, Addr, Din, Memory 314.)

c. conductors for providing an operand for the write operation to said one of the plurality of registers (Col. 12, lines 24 – 35, Fig. 6A, Data 304, Interconnect Bus 360/ The Interconnect Bus 360 provides data (an operand) for the write operation (write into local memory of participating node) to said one of the plurality of registers (memory blocks in distributed common memory).)

d. a set of broadcast specifiers; (Col. 12, lines 36 – 50/ Fig. 6A, System to Local Part. Ram 319B, Local to System Part Ram. 319A/ Each partition RAMs is a set of broadcast specifiers.)

e. compare circuitry for comparing the one of the plurality of registers and a selected one of the broadcast specifiers (Col. 12, lines 10 – 45/ Fig. 6A, Address Translation Hardware 319, System to Local Part. Ram 319B and Local to System Part. Ram 319A/ A selected one of the broadcast specifiers is an entry in the partition RAMs. A memory block, indexed by an address, is the one of the plurality of registers where data is written. The Address Translation Hardware 319 contains the partition tables, whose entries are accessed with an address, is the compare circuitry for comparing the one of the plurality of registers (by its address) and a selected one of the broadcast specifiers. (partition RAM entries))

f. and for providing a broadcast enable signal; and (Fig. 7/ Col. 12, lines 45 – 50, 61 - 65, Col. 13, lines 7 - 15) / Fig. 7 also illustrates an example of distributed common memory. The entry in the partition RAMs contains information regarding whether the entry is valid and, thus allows the memory write to be transacted on the system bus. This is used to by the hardware routing logic to determine whether the local memory write is translated into a system memory write. The hardware routing logic that allows the local memory write to be forwarded to other nodes via the system interconnect bus is providing a broadcast enable signal.)

g. a port, coupled to the compare circuitry, for communicating with a coprocessor communication bus, said port comprising at least one coprocessor communication bus

signal for selectively providing said operand in response to the broadcast enable signal (Col. 12, lines 16 – 35, Col. 13, lines 7 - 15/ Fig. 6A, Bus Interface 317, Interconnect Bus 360/ The port is the Bus Interface 317. It is coupled to the Address Translation Hardware 319. The coprocessor communication bus is the Interconnect Bus 360. The Bus Interface 317 communicates the translated system address and data to the coprocessor communication bus. It broadcasts a write operation with data when the Address Translation Hardware allows the write transfer to be forwarded to other nodes, which is selectively broadcasting said operand in response to the broadcast enable signal.)

27. Referring to claim 11, Parrish et al. have taught the processor of claim 10, as described above, and wherein each broadcast specifier within the set of broadcast specifiers comprises a set of broadcast indicators. (Col. 12, lines 13 – 35, lines 45 – 50, Fig. 6A, System to Local Part. Ram 319B, Local to System Part. Ram 319A, wire 305/ Each partition RAMs is a set of broadcast specifiers An entry in a partition RAMs is a broadcast specifier. The fourteen most significant bits of the address provided by the partition RAMs is the broadcast indicator.)

28. Referring to claim 12, Parrish et al. have taught the processor of claim 11, as described above, and wherein each broadcast indicator corresponds to at least one of the plurality of registers.(Col. 12, lines 13 – 35, lines 45 – 50, Fig. 6A, System to Local Part. Ram 319B, Local to System Part. Ram 319A, wire 305/ The fourteen most significant bits of the address provided by the partition RAMs is the broadcast indicator. The fourteen most significant bits of the address correspond to memory blocks, at least one of the plurality of registers.)

29. Claims 10 and 13-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Steinmetz et al. (US Pat. 5,485,624).

30. Referring to claim 18, Steinmetz et al. have taught (Please note claim objection above regarding the interpretation of the compare circuitry.) a processor, comprising:

a. a plurality of registers (Col. 3, lines 26 – 37, Col. 3 lines 38, "Fig.4 shows registers within DMA registers 23." Fig. 3, DMA Registers 23, Fig. 4/ The DMA registers are a plurality of registers.)

b. conductors for providing an operand for the write operation to said one of the plurality of registers; (Col. 3, lines 26 – 37, Fig. 3, Data Bus 12, DMA Registers 23/ Data bus 12 is coupled to DMA Registers 23. Data Bus 12 (conductors) provides data (providing an operand) that is loaded into DMA Registers 23 (for the write operation to said one of the plurality of registers).)

c. a program counter unit, for indicating address locations. (Col. 5, lines 7 – 67, Col. 6, lines 1 – 27, Col. 5 lines 56 – 59, Fig. 2/ The program counter unit is the program counter from Processor 14. The program counter unit indicates the address to be fetched. The processor uses the address from the program counter and places it on Address Bus 13.)

d. an execution region control unit, coupled to the program counter unit, for indicating when the indicated address from the program counter unit falls within one of a set of execution regions; and (Col. 2, lines 65 – 67, Col. 3, lines 1 – 37, Col. 3, lines 65 – 67, Col. 4, lines 1 – 19, Col. 5, lines 56 – 58, Fig. 3, Instruction Address Decoder 21, Control Signals 29, State Machine 22, Control Signals 26, Fig. 5/ The execution region control is the Instruction Address Decoder 21, Control Signals 29, State Machine 22, and Control Signals 26. The execution region control unit is coupled to the program counter

unit (Col. 5, lines 56 – 58), which supplies the address through the Address Bus 13. Instruction Address Decoder 21 produces Control Signal 29. Control Signal 29 includes snoop1 input 31, snoop2 input 32, snoop3 input, and qualifying control parameter (STERM) input 34. Sterm input 34 is asserted when address line A19 from address bus 13 is asserted. Snoop1 – Snoop3 input are asserted if A19 is asserted and selected combinations of A17-A18 from address bus 13 are asserted. The indicated address location is A17 – A19. Different combinations of A17 – A19, define the execution regions. The Control Signals 29, through the individual assertion of Snoop1 – Snoop3 inputs, indicate when A17-A19 (the indicated address location from the program counter unit) falls within one of a set of execution regions (defined by the selected combinations of A17 – A19).)

d. a port, coupled to the execution region control, for communicating with a coprocessor communication bus, (Col. 3, lines 21 – 37, Col. 6, lines 20 – 27, Fig. 2, Local Memory 10, Bus 6, Fig. 3, Data Bus 12, Address Bus 13, DMA Registers 23, DMA Controller 24/ DMA Register 23 and DMA Controller 24, the port, are coupled to the Instruction/ Address Decoder 21 and State Machine 26, the execution region control. The coprocessor communication bus is data bus 12 and address bus 13. The DMA Controller 24 oversees the DMA transfer between local memory 10 and bus 6 by reserving and releasing address bus 13 and data bus 12, and thus communicates with a coprocessor communication bus.)

e. said port comprising at least one coprocessor communication bus signal indicating a current execution region from the set of execution regions when the indicated address

location falls within one of the set of execution regions. (Col. 3, lines 65 – 67, Col. 4, lines 1 – 19, Col. 6, lines 20 – 27, Fig. 3/ The DMA Controller 24, the port, locks out Processor 14 from using Address Bus 13 and Data Bus 12. The DMA Controller is coupled to Processor 14 by Address Bus 13 and Data Bus 14, the coprocessor communication bus. Therefore, the mechanism in which the DMA Controller 24 locks out Processor 14 is the one coprocessor communication bus signal. A current execution region from the set of execution regions is the region defined by the address on the Address Bus 13. The DMA transfer is initiated by address bit A19 being asserted along with different combinations of address bits A17 – A18, which occurs because indicated address locations falls within one of the set of execution regions. The one coprocessor communication bus signal indicates a DMA transfer will occur, which is the result of the initiation of the DMA transfer by A17 – A19 being asserted.)

31. Although Steinmetz et al. teaches loading data into a DMA register (Col. 3, lines 26 – 33), Steinmetz et al. is silent regarding circuitry for performing a write operation to one of the plurality of registers. However, this feature is deemed to be inherent because data from the data bus is loaded into the selected DMA register. The Steinmetz et al. system would be inoperative if there was no circuitry for loading the data into the DMA register. The loading of data into the selected DMA register is performing a write operation to one of the plurality of registers.

32. Referring to claim 19, Steinmetz et al. have taught the processor of claim 18, as described above, and wherein said port further comprises:

a. at least one coprocessor communication bus signal for selectively providing said operand to be written to said one of the plurality of registers during said write operation

based on current execution region. (Steinmetz et al., Col. 21 – 37, Fig. 3, Data Bus 12, DMA Registers 23 / The said operand to be written to said one of the plurality of registers is the data from Data Bus 12 that is written, or loaded, into the DMA registers. The said write operation is the loading of data into a selected DMA register. This is done when the appropriate address bits are asserted, and thus, based on the current execution region. The coprocessor communication signal for selectively providing said operand is Data Bus 12, which is coupled to DMA Registers 23, for providing data that is loaded into the DMA registers.)

33. Referring to claim 20, Steinmetz et al. have taught the processor of claim 18, as described above, and wherein the execution region control unit comprises a plurality of region storage devices, wherein each execution region within the set of execution regions has a corresponding storage device for defining the execution region. (Col. 4, lines 65 – 67, Col. 5, lines 1 – 20, Fig. 3, State Machine 22, Fig. 5, State Machine 22, Fig. 6/ The State Machine 22 is part of the execution region control unit, and is the region storage device. It outputs signals depending on the address lines asserted, and thus, defines the execution regions.)

34. Referring to claim 10, Steinmetz et al. have taught a processor, comprising:

a. a plurality of registers (Fig. 1, Host Memory 20/ Host Memory 20, divided by its memory address, is a plurality of registers.)

b. conductors for providing an operand for the write operation to said one of the plurality of registers (Col. 2, lines 65 – 66, Col. 3, lines 38 – 64, Fig. 1, EISA I/O Bus 6 / During a DMA Read operation, data is transferred from I/O Device 3 to Host Memory 2 via EISA I/O Bus 6. The data is written into Host Memory 2 starting at the host address.

The EISA I/O Bus 6, (conductors) provides data (for providing an operand) to be written into Host Memory 2 starting at the host address (for the write operation to said one of the plurality of registers.)

c. a set of broadcast specifiers; (Col. 3, lines 59 – 64, Fig. 4, write DMA count (WDC) register 44, write control (WC) register 45, / The WDC register and WC register are a set of broadcast specifiers. They contain information regarding the start and length of the DMA transfer.)

d. compare circuitry for comparing the one of the plurality of registers and a selected one of the broadcast specifiers and for providing a broadcast enable signal; and (Col. 3, lines 38 – 67, Col. 6, lines 20 – 27, Fig. 3, DMA Registers 23, DMA Controller 24, Fig. 4, Write EISA base address lower (WEBAL) register 41, write EISA base address upper (WEBAU) 42, Write Control (WC) Register 45/ The one of the plurality of registers is located at the start address for the DMA transaction. The start address of one of the plurality of registers is a concatenation of the WEBAU and WEBAL registers. A selected one of the broadcast specifiers is the WC register. Once the WC register is set, the DMA Controller 24 initiates the DMA transaction starting at the host address. The DMA Controller 24 is the compare circuitry for comparing the one of the plurality of registers and a selected one of the broadcast specifiers. The broadcast enable signal is the start bit and the lock-out bit.)

e. a port, coupled to the compare circuitry, for communicating with a coprocessor communication bus, (Col. 3, lines 60 – 64, Fig. 3, DMA Controller 24, Data Bus 12, Address Bus 13/ The DMA Controller is the port. It is coupled to the compare circuitry,

itself. The coprocessor communication bus is Data Bus 12 and Address Bus 13. The DMA Controller 24 initiates the DMA transaction over the Data Bus 12 and Address Bus 13, and thus communicates with a coprocessor communication bus.).

f. said port comprising at least one coprocessor communication bus signal for selectively providing said operand in response to the broadcast enable signal. (Col.3, lines 47 – 50, Col. 6, lines 21 – 28/ The said port is the DMA Controller 24. The coprocessor communication bus is the Address Bus 13 and Data Bus 12. DMA Controller 24 first locks out Processor 14 from using the bus by the broadcast enable signal, and then initiates a DMA transaction, which includes DMA reads. A DMA read transaction reads data from an I/O device 3 and writes it into Host Memory 2. The data written into Host Memory 2 is said operand, which is driven over Data Bus 12.)

35. Steinmetz et al. is silent regarding circuitry for performing a write operation to one of the plurality of registers. However, this feature is deemed to be inherent to the Steinmetz et al. system because, for a DMA read operation, data is transferred from I/O Device 3 to Host Memory 2 over EISA I/O Bus 6 (Col. 2, lines 65 – 66, Col. 3, lines 52 – 56). The Steinmetz et al. system would be inoperative if there was no circuitry to write data into memory because the DMA read operation would not work.

36. Claim 13 does not recite limitations above the claimed invention set forth in claim 18 and is therefore rejected for the same reasons set forth in the rejection of claim 18 above.

37. Claim 14 does not recite limitations above the claimed invention set forth in claim 18 and is therefore rejected for the same reasons set forth in the rejection of claim 18 above.

38. Claim 15 does not recite limitations above the claimed invention set forth in claim 20 and is therefore rejected for the same reasons set forth in the rejection of claim 20 above.

39. Referring to claim 16, Steinmetz et al. have taught the processor of claim 15, as described above, and wherein each region storage device comprises an upper bound storage device (Col. 4, line 65 – Col. 6, line 28, Upper combination of A17-A19) and a lower bound storage device to define each broadcast region (Col. 4, line 65 – Col. 6, line 28, lower combination of A17-A19).

40. Referring to claim 17, Steinmetz et al. have taught the processor of claim 15, as described above, and wherein each region storage device comprises a base location storage device (Col. 4, line 65 – Col. 6, line 28, A17, A18, or A19) and a mask storage device to define each broadcast region (Col. 4, line 65 – Col. 6, line 28, High order bits are masked out in order to operate on the low order sixteen bits for each broadcast region.).

Conclusion

41. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tonia L Meonske whose telephone number is (703) 305-3993. The examiner can normally be reached on Monday-Friday, 8-4:30.

42. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie P Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

43. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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